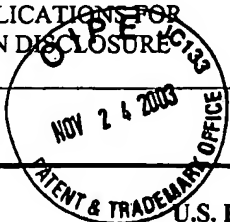


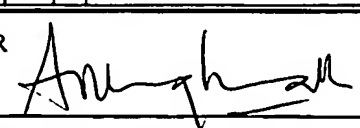
SUPPLEMENTAL FORM PTO-1449 (Modified)			ATTY. DOCKET NO. BUR920030096US1		SERIAL NO. Unassigned 10/707,069	
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT			APPLICANT: Steven H. Voldman			
(Use several sheets if necessary)			FILING DATE: Concurrently Herewith		GROUP: Unassigned 2825	



REFERENCE DESIGNATION							
U.S. PATENT DOCUMENTS							
EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)	

FOREIGN PATENT DOCUMENTS							
DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION		
					YES	NO	

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
NMD		T. Aoki, "A Practical High-Latchup Immunity Design Methodology for Internal Circuits in the Standard Cell-Based CMOS/BiCMOS LSI's", IEEE Transactions on Electron Devices, Vol. 40, No. 8, August 1993.
NMD		B. Basaran, et al., "Latchup-Aware Placement and Parasitic-Bounded Routing of Custom Analog Cells", IEEE, 1993.
NMD		H. de La Rochette, et al., "The Effect of Layout Modification on Latchup Triggering in CMOS by Experimental and Simulation Approaches", IEEE Transactions on Nuclear Science, Vol. 41, No. 6, December 1994.
NMD		S. Bhattacharya, et al., "Design Issues for Achieving Latchup-free, Deep Trench-Isolated, Bulk, Non-Epitaxial, Submicron CMOS", IEDM, 1990.
NMD		M. Ker, et al., "New Experimental Methodology to Extract Compact Layout Rules for Latchup Prevention in Bulk CMOS IC's", IEEE Custom Integrated Circuits Conference, 1999.
NMD		M. Ker, et al., "Layout Design and Verification for Cell Library to Improve ESD/Latchup Reliability in Deep-Submicron CMOS Technology", IEEE Custom Integrated Circuits Conference 1998.


EXAMINER 	DATE CONSIDERED 09/21/05
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	METHODOLOGY FOR PLACEMENT BASED ON CIRCUIT FUNCTION AND LATCHUP SENSITIVITY						
<p>Application Number : 10/707,069</p> <p>Confirmation Number:</p> <p>First Named Applicant: Steven Voldman</p> <p>Attorney Docket Number: BUR920030096US1</p> <p>Art Unit: 2825</p> <p>Examiner: DORF, NEHIA</p> <p>Search string: (5796638 or 6086627 or 20020144213 or 20020040985).pn</p>							
US Patent Documents							
Note: Applicant is not required to submit a paper copy of cited US Patent Documents							
init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
NMD	1	5796638	1998-08-18	Kang et al.			
NMD	2	6086627	2000-07-11	Bass Jr. et al.			
US Published Applications							
Note: Applicant is not required to submit a paper copy of cited US Published Applications							
init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
NMD	1	20020144213	2002-10-03	Ramaswamy et al.			
NMD	2	20020040985	2002-04-11	Aldrich			
Signature							
Examiner Name				Date			
				07/21/05			